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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/731,385	12/06/2000	Myeong-cheol Kim	SAM-164	8322

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EXAMINER	
NADAV, ORI	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 01/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/731,385	KIM ET AL.	
	Examiner	Art Unit	
	ori nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 14-40* is/are pending in the application.

4a) Of the above claim(s) *16-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,14,15 and 21-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-7, 14-15, 21-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner et al. (5,882,973) in view of Nguyen (6,472,261) and Huang (5,899,722).

Regarding claims 1, 21 and 31, Gardner et al. teach in figure 7 and related text a semiconductor device comprising:

a plurality of conductive patterns 18a, 18b formed to be adjacent to one an other by sequentially stacking and patterning a first conductive layer 18 on a particular underlying layer 10;

a first insulation layer (the small square under layer 28b) filling a gap between adjacent conductive patterns the first insulation layer being formed of a first insulating material (silicon oxide) and being formed laterally adjacent to and not underneath the conductive patterns,

a second insulation layer 28b having a spacer shape, the second insulation layer formed at the sides of each conductive pattern and over the first insulation layer; the

second insulation layer being formed of a second insulating material (silicon nitride) different from the first insulating material, and

a second conductive layer 48 being a single uninterrupted layer and having a contact portion that fills a contact hole which is self-aligned with respect to the second insulation layer between adjacent conductive patterns, the contact hole passing through the first insulation layer, the first insulation layer extending between adjacent conductive patterns and between the second conductive layer and the conductive patterns and having a single aligned planar top surface throughout the distance between at least one of the conductive patterns and the second conductive layer, and

third insulation layer (located between layer 28b and 18b) provided between the first insulation layer and the sides of each conductive layer pattern and between the second insulation layer and the side of the conductive layer pattern,

wherein the third insulation layer provided on the surfaces of the conductive pattern and on the surface of the underlying layer and being absent from a portion of the underlying layer that contacts the second conductive layer.

Gardner et al. do not teach a second conductive layer being formed over the conductive patterns, and do not explicitly state that the contact between the plurality of conductive patterns 18a, 18b is a self-aligned contact formed by sequentially stacking and patterning a first conductive layer and a mask layer.

Nguyen teaches in figure 6 and related text a semiconductor device having a self-aligned contact, wherein the semiconductor device comprising a plurality of conductive patterns formed to be adjacent to one an other by sequentially stacking and patterning a

first conductive layer 14 and a mask layer 18, and a second conductive layer 42 filling a contact hole which is self-aligned with respect to the second insulation layer between adjacent conductive patterns, the contact hole passing through the first insulation layer. Huang teaches in figure 2 a second conductive layer 17 being a single uninterrupted layer formed over conductive patterns and having a contact portion that fills a contact hole.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the second conductive layer over the conductive patterns, and to form the contact between the plurality of conductive patterns in Gardner et al.'s device to be a self-aligned contact by sequentially stacking and patterning a first conductive layer and a mask layer in order to form an operable device and in order to improve the processing steps of making the device. The combination is motivated by the teachings of Gardner et al. who point out that the structure depicted in figure 7 is not the final product, and metalizations and interlayer dielectrics are required to form an operable device (column 8, lines 9-19).

Regarding claims 2, 23 and 33, Gardner et al. teach in figure 7 a top of the first insulation layer is lower than the top of the first conductive layer 18a of each conductive layer pattern.

Regarding claims 3, 24 and 34, Gardner et al. do not teach in figure 7 the top of the first insulation layer is higher than the top of the first conductive layer. Nguyen teaches in

figure 6 the top of the first insulation layer 22 is higher than the top of the first conductive layer of each conductive layer pattern 14. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the top of the first insulation layer to be higher than the top of the first conductive layer in Gardner et al.'s device in order to provide better protection to the gate electrode.

Regarding claims 4-7, 25-28 and 35-38, Gardner et al. teach in figure 7 an etching rate of the first insulation layer is larger than that of the second insulation layer, the dielectric constant of the first insulation layer is smaller than that of the second insulation layer, wherein the first insulation layer is formed of a silicon oxide layer and the second insulation layer is formed of a silicon nitride layer.

Regarding claims 15, 30 and 40, Gardner et al. teach in figure 7 the first conductive layer of each conductive layer pattern is a gate electrode, and the contact contacts the surface of a semiconductor substrate.

Regarding claims 22 and 32, Gardner et al. do not teach that the third and fourth insulation layers are formed at a thickness of 50-200 A. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use third and fourth insulation layers at a thickness of 50-200 A in Gardner et al.'s device, in order to provide adequate insulation to the device and because it is well within the skills of an

artisan to optimize the performance of the device by forming the third and fourth insulation layers at the required thickness.

Regarding claims 14, 29 and 39, Gardner et al. do not teach using the first conductive layer of each conductive layer pattern as a bit line, and the second conductive layer to connect a storage electrode of a semiconductor capacitor to a semiconductor substrate.

Huang teaches that a self aligned contact structure, similar to that disclosed by Chang et al., can be used in a DRAM. A DRAM comprises a first conductive layer being a bit line, and a second conductive layer serves to connect a storage electrode of a semiconductor capacitor to a semiconductor substrate. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Gardner et al. and Nguyen's device in a DRAM device in order to use the device in a specific application which requires a DRAM device. Note that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

Response to Arguments

Applicant's arguments with respect to claims 1-7, 14-15 and 21-40 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(571) 272-1660**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

O.N.
December 31, 2004

ORI NADAV
PRIMARY EXAMINER
TECHNOLOGY CENTER 2800